AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A programmable logic device, comprising:

configurable logic blocks, the configurable logic blocks configured to provide a multi-stage crossbar switch;

the multi-stage crossbar switch including:

a first stage configured from a first portion of the configurable logic blocks to provide a first plurality of crossbars, the first stage having inputs;

a second stage configured from a second portion of the configurable logic blocks to provide a second plurality of crossbars;

a third stage configured from a third portion of the configurable logic blocks to provide a third plurality of crossbars, the third stage having outputs;

first interconnects for coupling the first plurality of crossbars to the second plurality of crossbars; and

second interconnects for coupling the second plurality of crossbars to the third plurality of crossbars;

wherein the inputs and the outputs are selectable via reconfiguration while concurrently operating at least part of the multi-stage crossbar switch for responsive path configuration to provide input-to-output cross-connectivity via the first stage, the second stage and the third stage using the first interconnects and the second interconnects;

wherein latency from any of the inputs cross-connected to any of the outputs is a same number of clock cycles without having to provide delay compensation.

2. (Original) The programmable logic device, according to claim 1, wherein the first plurality of crossbars is for receiving input data, and wherein the third plurality of crossbars is for outputting the input data.

3. (Original) The programmable logic device, according to claim 2, wherein the

first plurality of crossbars are interleaved with the third plurality of crossbars.

4. (Original) The programmable logic device, according to claim 2, wherein the first interconnects and the second interconnects are disposed in an interconnect region, and wherein the second plurality of crossbars are disposed within the interconnect region.

5. (Original) The programmable logic device, according to claim 4, wherein the first plurality of crossbars and the third plurality of crossbars are not disposed within the interconnect region.

6. (Original) The programmable logic device, according to claim 4, wherein the second plurality of crossbars are arrayed.

7. (Original) The programmable logic device, according to claim 1, wherein each crossbar of the first plurality of crossbars comprise:

a first set of the first portion of the configurable logic blocks configured to provide input flip-flops; and

a second set of the first portion of the configurable logic blocks configured to provide multiplexers and output flip-flops.

8. (Original) The programmable logic device, according to claim 7, wherein outputs of the input flip-flops are selectively coupled to and uncoupled from function generators through partial reconfiguration.

9. (Original) The programmable logic device, according to claim 7, further comprising:

double-length lines connected to the outputs of the input flip-flops; and

programmable input select circuitry configured to selectively couple and uncouple function generators to and from the double-length lines.

10. (Original) The programmable logic device, according to claim 1, wherein each crossbar of the first plurality of crossbars, the second plurality of crossbars and the third plurality of crossbars comprises:

at least one configurable logic block configured to provide at least one input register; and

at least one other configurable logic block configured to provide at least one multiplexer, the at least one multiplexer coupled to the at least one input register.

11. (Original) The programmable logic device, according to claim 1, wherein each crossbar of the first plurality of crossbars, the second plurality of crossbars and the third plurality of crossbars pipelines data from an input register stage to a multiplexer stage and to an output register stage for three stage intra-crossbar processing.

12. (Original) The programmable logic device, according to claim 11, wherein the input register stage comprises at least one configurable logic block configured to provide an input flip-flop.

13. (Original) The programmable logic device, according to claim 12, wherein the multiplexer stage comprises at least one other configurable logic block configured to provide at least one multiplexer, the at least one multiplexer coupled to the at least one input register.

14. (Original) The programmable logic device, according to claim 13, wherein the data passes through the input flip-flop, the at least one multiplexer and an output flip-flop for the three stage intra-crossbar processing.

15. (Original) The programmable logic device, according to claim 14, wherein output of the at least one multiplexer is coupled as input to at least one other multiplexer for the three stage intra-crossbar processing for the third plurality of

crossbars.

16. (Original) The programmable logic device, according to claim 1, wherein each crossbar of the second plurality of crossbars comprises:

a first set of the second portion of the configurable logic blocks configured to provide input flip-flops; and

a second set of the second portion of the configurable logic blocks configured to provide multiplexers and output flip-flops.

17. (Original) The programmable logic device, according to claim 16, wherein outputs of the input flip-flops are selectively coupled to and uncoupled from lookup tables through partial reconfiguration.

18. (Original) The programmable logic device, according to claim 16, further comprising:

double-length lines connected to the outputs of the input flip-flops; and

programmable input select circuitry configured to selectively couple and uncouple to lookup tables and from the double-length lines.

19. (Original) The programmable logic device, according to claim 1, wherein each crossbar of the third plurality of crossbars comprise:

a first set of the third portion of the configurable logic blocks configured to provide input flip-flops; and

a second set of the third portion of the configurable logic blocks configured to provide multiplexers and output flip-flops.

20. (Original) The programmable logic device, according to claim 19, wherein outputs of the input flip-flops are selectively coupled to and uncoupled from the lookup tables through partial reconfiguration.

21. (Original) The programmable logic device, according to claim 19, further comprising:

double-length lines connected to outputs of the input flip-flops; and

programmable input select circuitry connected to the double-length lines for selectively coupling and uncoupling lookup tables to and from the double-length lines.

22. (Currently Amended) A method for providing a crossbar switch, comprising:

providing a first portion of configurable logic configurable to provide a first stage of crossbars;

providing a second portion of configurable logic configurable to provide a second stage of crossbars;

providing a third portion of configurable logic configurable to provide a third stage of crossbars; and

partially reconfiguring at least one of the first, second and third stage of crossbars to provide an input-to-output cross-connection from input of the first portion of the configurable logic to output of the third portion of the configurable logic via the first, second and third portion of configurable logic;

wherein latency from any of the input of the first portion cross-connected to any of the output of the third portion is a same number of clock cycles without having to provide delay compensation.

23. (Original) The method, according to claim 22, wherein the partially reconfiguring comprises partial reconfiguration of a crossbar from each of the first stage of crossbars, the second stage of crossbars and the third stage of crossbars to provide the input-to-output cross-connection.

24. (Original) The method, according to claim 22, wherein the partial reconfiguring comprises partial reconfiguration of a crossbar from each of the first stage of crossbars and the third stage of crossbars to provide the input-to-output cross-connection.

25. (Original) The method, according to claim 22, wherein the partial reconfiguring is done while operating the crossbar switch.

26. (Original) The method, according to claim 22, wherein the partial reconfiguring does not affect operations in a fourth portion of the configurable logic not used in the partial reconfiguring.

27. (Original) The method, according to claim 22, wherein the crossbar switch is instantiated in a field programmable gate array ("FPGA"), the FPGA having a processor, a port and internal memory, the partial reconfiguring being done entirely on the FPGA by:

accessing via the port configuration information stored in the memory;

modifying the configuration information stored in the internal memory with the processor; and

writing via the port the configuration information as modified to dynamically reconfigure the configurable logic.

28. (Currently Amended) A crossbar switch for a programmable logic device, comprising:

input pins and output pins, each input pin being connectable to each output pin for cross-connectivity through an odd number of crossbar stages greater than one, the crossbar stages provided by configurable circuitry configured to provide crossbars, the cross-connectivity reconfigurable responsive to user programming to indicate which input pins are to be cross-connected to which output pins for the crossbars instantiated in the programmable logic device, wherein the crossbar stages instantiated are partially reconfigured to provide the cross-connectivity responsive to the user programming while maintaining operation of a portion of the crossbar stages;

wherein latency from any of the input pins cross-connected to any of the output pins is a same number of clock cycles without having to provide delay compensation.

29. (Original) The crossbar switch, according to claim 28, wherein each of the crossbars is provided in part using selectors and function generators, the selectors being under configuration bit control.

Claim 30. (Cancelled).

31. (Currently Amended) A crossbar switch kit, comprising:

a programmable logic device including configurable circuitry; and

configuration information for configuring the programmable logic device as a crossbar switch, the crossbar switch having input pins and output pins, each input pin being connectable to each output pin for cross-connectivity through an odd number of crossbar stages equal to or greater than three, the crossbar stages provided by configuring the configurable circuitry to provide crossbars, wherein the crossbars instantiated are reconfigurable to provide the cross-connectivity while maintaining operation of circuitry of the crossbars unaffected by reconfiguration;

wherein latency from any of the input pins cross-connected to any of the output pins is a same number of clock cycles without having to provide delay compensation.

32. (Previously Presented) The crossbar switch kit, according to claim 31, wherein the cross-connectivity is user determinable by selecting an input pin of the input pins to be cross-connected to a respective output pin.

33. (Original) The crossbar switch kit, according to claim 31, wherein the cross-connectivity is user determinable by selecting an input pin of the input pins to be cross-connected to a plurality of the output pins.

34. (Currently Amended) A method for instantiating a crossbar switch in a programmable logic device, comprising:

providing predefined configuration bits for the instantiating of the crossbar infrastructure in the programmable logic device, the crossbar infrastructure including at

least three crossbar stages; and

providing user access to select one or more inputs and outputs of the crossbar infrastructure for responsively configuring path cross connectivity, wherein at least part of the crossbar infrastructure is concurrently operated while another part is being reconfigured to provide the path cross connectivity;

wherein latency from any of the inputs cross-connected to any of the outputs is a same number of clock cycles without having to provide delay compensation.

35. (Original) The method, according to claim 34, wherein the user access comprises user definable configuration bit control for selection of the one or more inputs and outputs, the path cross connectivity configured responsive to the user definable configuration bit control.

36. (Currently Amended) An integrated circuit comprising:

configurable logic blocks, the configurable logic blocks configured to provide a multi-stage crossbar switch;

the multi-stage crossbar switch including:

a first stage configured from a first portion of the configurable logic blocks to provide a first plurality of crossbars, the first stage having inputs;

a second stage configured from a second portion of the configurable logic blocks to provide a second plurality of crossbars;

a third stage configured from a third portion of the configurable logic blocks to provide a third plurality of crossbars, the third stage having outputs;

first interconnects for coupling the first plurality of crossbars to the second plurality of crossbars; and

second interconnects for coupling the second plurality of crossbars to the third plurality of crossbars; and

an embedded processor operably configured to reconfigure at least one of the first, second, or third stages while maintaining operation of at least a portion of the multi-stage crossbar switch unaffected by reconfiguration;

wherein latency from any of the inputs cross-connected to any of the outputs is

a same number of clock cycles without having to provide delay compensation.

37. (Original) The integrated circuit of claim 36 wherein the first and third stages are dynamically reconfigured.

38. (Currently Amended) ~~An integrated circuit~~ A programmable logic device comprising:

a crossbar switch having configurable logic blocks[[;]], wherein the crossbar switch is a multistage crossbar switch having configurable interconnects coupling inputs of the multistage crossbar switch to outputs of the multi-stage crossbar switch;

an embedded processor operably configured to reconfigure the crossbar switch while maintaining operation of at least a portion of the crossbar switch unaffected by reconfiguration;

wherein latency from any of the inputs cross-connected to any of the outputs is a same number of clock cycles without having to provide delay compensation.

Claim 39. (Cancelled).

40. (Currently Amended) The programmable logic device ~~integrated circuit~~ of claim 38 wherein the embedded processor includes a soft-core or a hard-core processor.

41. (Currently Amended) The programmable logic device ~~integrated circuit~~ of claim 38 wherein the embedded processor is a circuit selected from a group consisting of a digital signal processor, a general-purpose processor, an application specific processor, and customized digital logic.